4GHz Miniaturized Low Noise Dielectric Resonator Stabilized Oscillator

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Abstract

A 4GHz Miniaturized Oscillator has been developed. It consists of a 17GHz (17.84GHz) DRO and a divide-by-four analog frequency divider. The 17GHz DRO uses a HEMT with series feedback. The frequency divider was built, based on the concept of an injection locking oscillator using a bipolar transistor. The circuit provides excellent phase noise of - 120dBc/Hz at 100kHz offset from the carrier and good temperature stability of +/- 150KHz over the temperature range -20°C to +80°C. The circuit size is about 1/8 that of a conventional 4.46GHz DRO.

Introduction

Recently, the need to develop a small and excellent phase noise oscillator for microwave measurement instruments such as spectrum analyzers used for mobile radio and microwave link maintenance is increasing. A dielectric stabilized oscillator has been chosen for that application. A Dielectric Resonator is preferable for oscillators because of its small size, high unloaded Q and excellent integrability.

However, since the operating frequency is not so high, the DRO housing becomes large. For instance, the approximate dimensions, dielectric constant and unloaded Q for a 4.46GHz operating frequency are dr=0.5 inches (12.7mm) tr=0.22 inches (5.6mm), Er=38 and Q=10000, respectively.

If a high DR is chosen, its approximate dimensions, dielectric constant and Q value are dr=0.38 inches (9.7mm), Lr=0.15 inches (3.81mm), Er=80 and Q=3000. For small size oscillator requirements, the dimensions of the DR is critical. Because the DRO housing is decided by the dimension of the DR. A high dielectric constant provides the added benefit of size. As a result, unloaded Q is decreased and phase noise sacrificed. The 17GHz DRO and 1/4 analog frequency divider combination were used for the designed 4.46GHz oscillator. This approach the meets the requirements of small size and good phase noise. The dimensions of DR for a 17.84GHz operating frequency are about one fourth compared to a 4.46GHz DR. Also, 1/4 frequency division improves the phase noise of the DRO by 12dB.

Circuit Design

1. 17GHz DRO

The schematic circuit for the DRO is shown in Figure 1. Common gate inductive feedback was used because of its simplicity

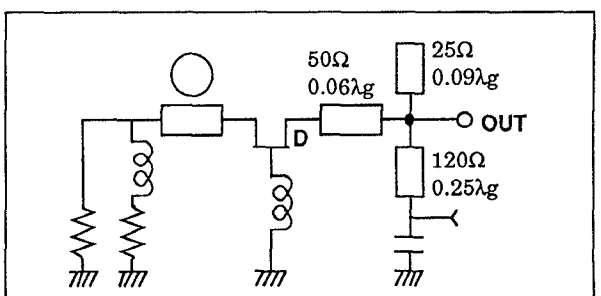

Fig.1 Schematic circuit diagram of 17GHz DRO

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and effective generation of strong negative resistance at a desired fixed frequency. And the active device is a 0.25μm HEMT chip with substantial gain and the power generating capability to drive a 1/4 frequency divider at 17.84GHz. A Fujitsu FHX30X was chosen for this application. An initial bias point of Vd=3V, Id=20mA was selected.

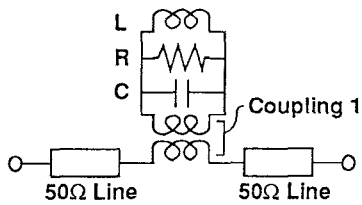

Fig. 2 Resonator equivalent circuit

The dielectric resonator is fabricated from Sumitomo metal mining SDR type material with a dielectric constant of 30. Its dimensions are dr=0.13 inches (3.3mm), Lr=0.06 inches (1.5mm). The required temperature coefficient, Tf, of the DR was identified by temperature cycling the DRO with a 0ppm/°C DR. The oscillator exhibited a temperature drift of -3.2ppm/°C. The DRO fitted with DR of Tf=+3ppm/°C. was chosen for the final version.

The resonator equivalent circuit is shown in Figure 2. The resonator equivalent circuit is calculated from its Q and frequency, and the assumed values are L=8.8pH, C=10pF and R=600Ω, respectively.

The common gate inductance of the circuit was examined and optimized to obtain maximum negative resistance using a linear simulation program Touchstone having this inductance value ,the resonator equivalent circuit and the S parameters of the device. Simulated reflection gain Γd (at the drain point) is about 40dB. Impedance is Zd = -50 -j0.8 ohms. Load termination then becomes approximately 18 + j0.8 ohms. The load frequency determining network was implemented by a 0.06 wavelength transmission line of 50 ohms and a 0.09 wavelength open stub of 25 ohms. This DRO circuit was fabricated in a microstrip on a 15 mil alumina substrate.

2. 1/4 frequency divider

The schematic diagram of the frequency divider is shown in Figure 3.

The 1/4 frequency divider circuit was designed using the oscillator design method. In short, the circuit produces free running oscillation at the idler frequency (nearly 1/4 of input frequency). The injecting signals for the 1/4 frequency divider are obtain from the 17.84GHz stabilized DRO output signal.

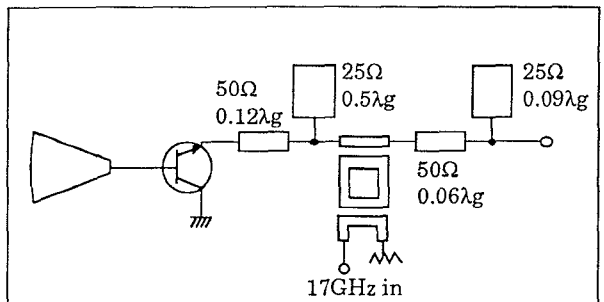

Fig. 3. Schematic circuit diagram of 1/4 frequency divider

The active device is a bipolar transistor (NEC NE64700). It has substantial gain at a 4.46GHz free running oscillation frequency. A radial stub was used for resonator circuit because of its broadband frequency characteristics. [1] And that resonator circuit was fabricated on a high dielectric constant material substrate Er=38, h=15 mil to minimize circuit size.

A traveling wave filter is used for injection of the 17.84GHz signal. The circuit has a matching network consisting of a 0.12 wavelength transmission line of 50 ohms and a 0.5 wavelength open stub of 25 ohms at 17.84GHz. The objective of this network is to achieve effective 17.84GHz input signal injection and obtain maximum negative resistance at a 4.46GHz idler frequency.

The frequency determining network has

matching for an imaginary impedance to zero at idler frequency. This matching network was implemented using a 0.06 wavelength transmission line of 50 ohms and a 0.09 wavelength open stub of 25 ohms at a 4.46GHz idler frequency.

The frequency divider circuit was fabricated on a 15 mil alumina substrate except for the resonator circuit.

Oscillator Performance

The 17GHz DRO, 1/4 frequency divider and their combined 4.46GHz low noise oscillator were implemented. Figure 4 shows a photo of the designed 4.46GHz low noise oscillator.

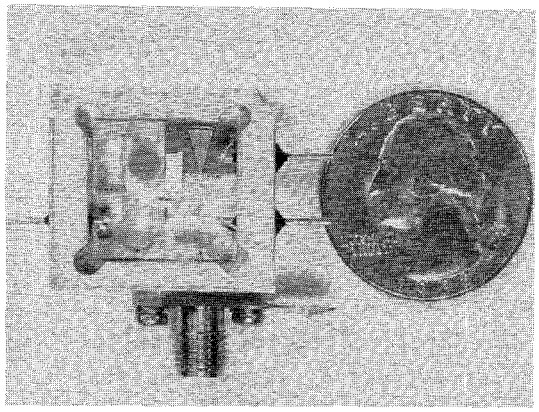

Fig. 4 Photo of the designed 4.46GHz oscillator

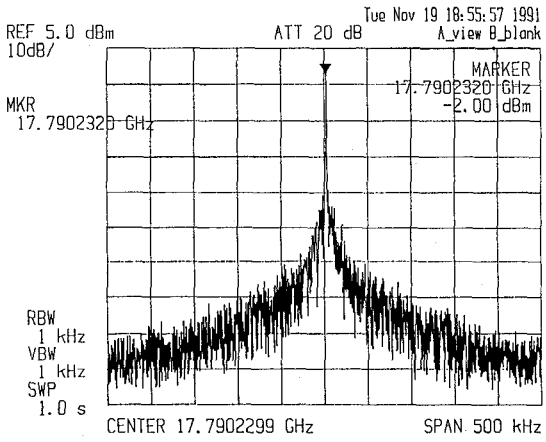

Fig. 5 Spectrum of the 17GHz DRO

The 17GHz DRO delivers 10dBm of output power at 17.84GHz. The spectrum of the 17GHz DRO is shown in Figure 5. The single sideband phase noise of the DRO was measured using an R3271 spectrum analyzer. At the frequency, the measurement limitations of the R3271 are about -100dBc/Hz at 10kHz offset and -113dBc/Hz at 100kHz offset. The phase noise is at -85 dBc/Hz at 10kHz offset and -108dBc/Hz at 100kHz offset.

The frequency division region of 1/4 frequency divider is shown in Figure 6. The locking bandwidth of about 200MHz was realized. Reducing the injected input level to -5 dBm resulted in a locking bandwidth of 10MHz. In this frequency divider, the minimum threshold signal input power was -12dBm. And this threshold signal level is dependent on the resonator's Q value.

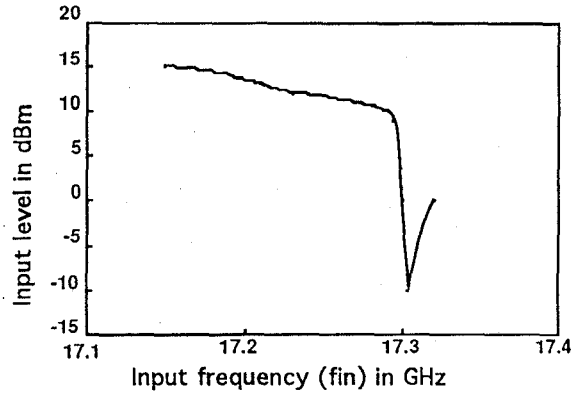

Fig. 6 Domain of frequency division

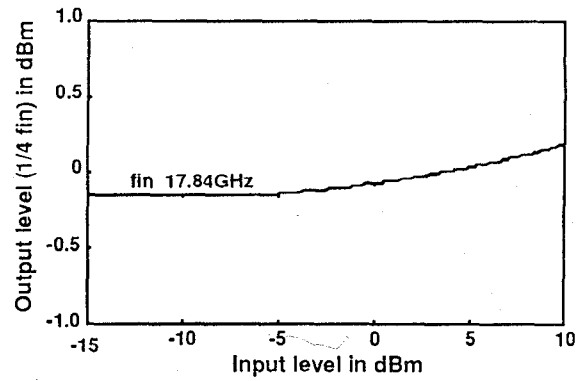

Fig. 7 Output level characteristics for a fixed fin

Figure 7 shows the Output level characteristics. The output level of the frequency divider is constant above the minimum threshold level.

Figure 8 shows the spurious characteristics. Good suppression of the 17.84GHz fundamental DRO signal was observed at the output. The spurious signal is nominally 23dB below the desired output signal.

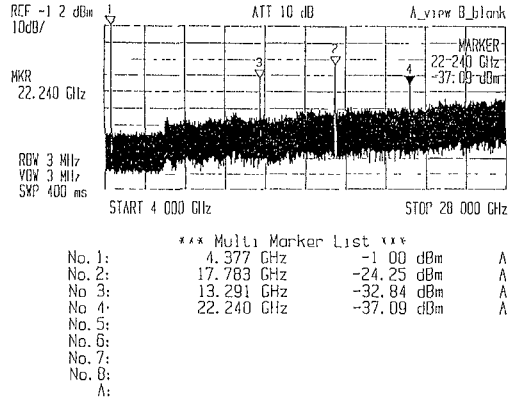

Fig. 8 Spurious characteristics

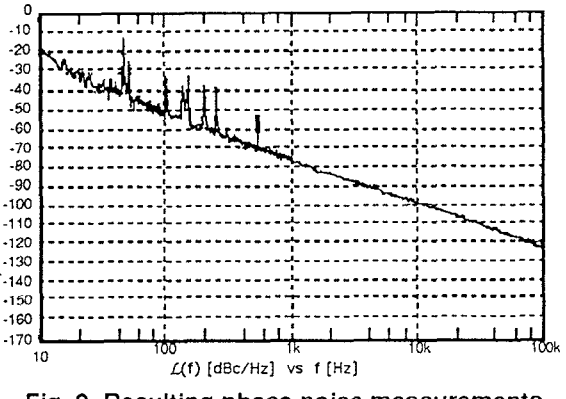

Fig. 9 Resulting phase noise measurements

The phase noise of the measured 4.46GHz oscillator is shown in Figure 9. The single sideband phase noise of the oscillator was measured using an HP3048A phase noise measurement system. The measured phase noise of the 4.46GHz output signal is about -100dBc/Hz at 10kHz offset and -120dBc/Hz at 100kHz offset.

The maximum frequency drift is within +/-150KHz for operation over the temperature range of -20°C to 80°C.

Conclusion

The 4GHz miniaturized oscillator has been developed using a 1/4 frequency divider which is based on an injection locking oscillator. With a volume of 1 x 0.8 x 0.44 inches (25.4 x 20.3 x 11.2 mm), a compact circuit compared with a conventional 4.4GHz DRO has been realized.

This experiment also shows that the DRO and frequency divider combination provides several advantages of small volume and ease of design.

Acknowledgments

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